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(54) A flexible high density interconnect structure and flexibly interconnected system.

(57) A flexible high density interconnect structure is provided by extending the high density interconnect structure beyond the solid substrate (14) containing the chips (20) interconnected thereby. During fabrication, the flexible portion (39) of the high density interconnect structure is supported by a temporary interconnect support to facilitate fabrication of the structure in accordance with existing fabrication techniques. Subsequently, that temporary support structure may be removed or may remain in place if it is sufficiently flexible to impart the desired degree of flexibility to that portion of the high density interconnect structure. Methods of fabrication are also disclosed.

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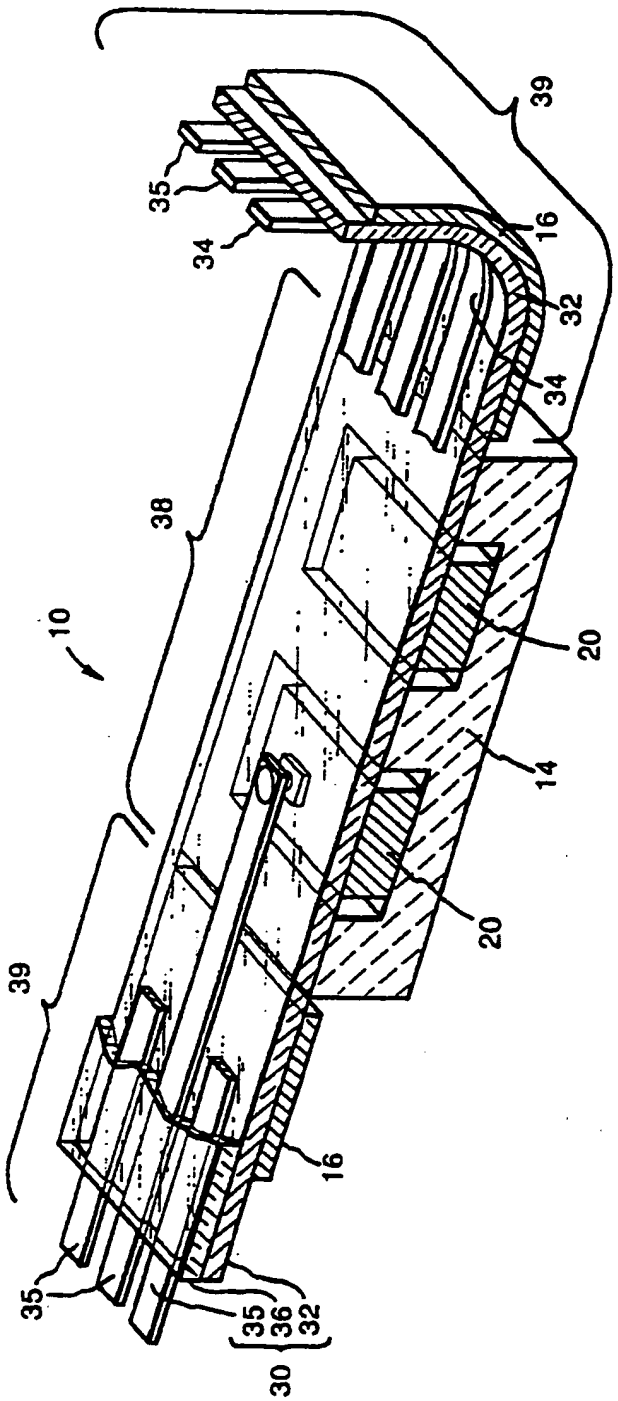
FIG. 1



The present invention relates to the field of multi-component or multi-chip circuits, and more particularly, to high density interconnection of multiple components or chips.

A high density interconnect (HDI) structure or system which has been developed by General Electric Company offers many advantages in the compact assembly of digital and other electronic systems. For example, an electronic system such as a micro computer which incorporates between 30 and 50 chips can be fully assembled and interconnected on a single substrate which is 2 inches long by 2 inches wide by .050 inch thick. The maximum operating frequency of such systems is normally, at present, less than about 50 MHz. Even more important than the compactness of this high density interconnect structure is the fact that it can be disassembled for repair or replacement of a faulty component and then reassembled without significant risk to the good components incorporated within the system. This reworkability or repairability is a substantial advance over prior connection systems in which reworking the system to replace damaged components was either impossible or involved substantial risk to the good components.

Briefly, in this high density interconnect structure, a ceramic substrate such as alumina which may be 100 mils thick and of appropriate size and strength for the overall system, is provided. This size is typically less than 2 inches square. Once the position of the various chips has been specified, individual cavities or one large cavity having appropriate depths at the intended locations of the various chips are prepared. This may be done by starting with a bare substrate having a uniform thickness and the desired size. Laser milling is used to form the cavities in which the various chips and other components will be positioned. For many systems where it is desired to place chips edge-to-edge, a single large cavity is satisfactory. That large cavity may typically have a uniform depth where the semiconductor chips have a substantially uniform thickness. Where a particularly thick or a particularly thin component will be placed, the cavity bottom may be made respectively deeper or shallower to place the upper surface of that component in substantially the same plane as the upper surface of the rest of the components and the surface of the portion of the substrate which surrounds the cavity. The bottom of the cavity is then provided with a thermoplastic adhesive layer which may-preferably be polyetherimide resin available under the trade name ULTEM® from the General Electric Company. The various componentsare then placed in their desired locations within the cavity, the entire structure is heated to the softening point of the ULTEM® polyetherimide (in the vicinity of 217°C to 235°C depending on the formulation used) and then cooled to thermoplastically bond the individual components to the cavity. At this stage, the upper surfaces of all components and the substrate are disposed in substantially a common plane. Thereafter, a polyimide film which may be Kapton® polyimide, available from E.I. du Pont de Nemours Company, which is about 0.0005-0.003 inch (12.5-75 microns) thick is pretreated to promote adhesion and coated on one side with an ULTEM® polyetherimide resin or another thermoplastic and laminated across the top of the chips, other components and the substrate with the ULTEM® resin serving as a thermoplastic adhesive to hold the Kapton® in place. Thereafter, via holes are laser drilled in the Kapton® and ULTEM® layers in alignment with the contact pads on the electronic components to which it is desired to make contact. A metallization layer which is deposited over the Kapton® layer extends into the via holes and makes electrical contact to the contact pads disposed thereunder. This metallization layer may be patterned to form individual conductors during the process of depositing it or may be deposited as a continuous layer and then patterned using photoresist and etching. The photoresist is preferably exposed using a laser to provide an accurately aligned conductor pattern at the end of the process.

Additional dielectric and metallization layers are provided as required in order to provide all of the desired electrical connections among the chips. Any miss-position of the individual electronic components and their contact pads is compensated for by an adaptive laser lithography system which is the subject of some of the U.S. Patents and Patent Applications which are listed hereinafter.

This high density interconnect structure, methods of fabricating it and tools for fabricating it are disclosed in U.S. Patent 4,783,695, entitled "Multichip Integrated Circuit Packaging Configuration and Method" by C.W. Eichelberger, et al.; U.S. Patent 4,835,704, entitled "Adaptive Lithography System to Provide High Density Interconnect" by C.W. Eichelberger, et al.; U.S. Patent 4,714,516, entitled "Method to Produce Via Holes in Polymer Dielectrics for Multiple Electronic Circuit Chip Packaging" by C.W. Eichelberger, et al.; U.S. Patent 4,780,177, entitled "Excimer Laser Patterning of a Novel Resist" by R.J. Wojnarowski et al.; U.S. Patent Application Serial No. 249,927, filed September 27, 1989, entitled "Method and Apparatus for Removing Components Bonded to a Substrate" by R.J. Wojnarowski, et al.; U.S. Patent Application Serial No. 310,149, filed February 14, 1989, entitled "Laser Beam Scanning Method for Forming Via Holes in Polymer Materials" by C.W. Eichelberger, et al.; U.S. Patent Application Serial No. 312,798, filed February 21, 1989, entitled "High Density Interconnect Thermoplastic Die Attach Material and Solvent Die Attachment Processing" by R.J. Wojnarowski, et al.; U.S. Patent Application Serial No. 283,095, filed December 12, 1988, entitled

"Simplified Method for Repair of High Density Interconnect Circuits" by C.W. Eichelberger, et al.; U.S. Patent Application Serial No. 305,314, filed February 3, 1989, entitled "Fabrication Process and Integrated Circuit Test Structure" by H.S. Cole, et al.; U.S. Patent Application Serial No. 250,010, filed September 27, 1988, entitled "High Density Interconnect With High Volumetric Efficiency" by C.W. Eichelberger, et al.; U.S. Patent Application Serial No. 329,478, filed March 28, 1989, entitled "Die Attachment Method for Use in High Density Interconnected Assemblies" by R.J. Wojnarowski, et al.; U.S. Patent Application Serial No. 253,020,filed October 4, 1988, entitled "Laser Interconnect Process" by H.S. Cole, et al.; U.S. Patent Application Serial No. 230,654, filed August 5, 1988, entitled "Method and Configuration for Testing Electronic Circuits and Integrated Circuit Chips Using a Removable Overlay Layer" by C.W. Eichelberger, et al.; U.S. Patent Application Serial No. 233,965, filed August 8, 1988, entitled "Direct Deposition of Metal Patterns for Use in Integrated Circuit Devices" by Y.S. Liu, et al.; U.S. Patent Application Serial No. 237,638, filed August 23, 1988, entitled "Method for Photopatterning Metallization Via UV Laser Ablation of the Activator" by Y.S. Liu, et al.; U.S. Patent Application Serial No. 237,685, filed August 25, 1988, entitled "Direct Writing of Refractory Metal Lines for Use in Integrated Circuit Devices" by Y.S. Liu, et al.; U.S. Patent Application Serial No. 240,367, filed August 30, 1988, entitled "Method and Apparatus for Packaging Integrated Circuit Chips Employing a Polymer Film Overlay Layer" by C.W. Eichelberger, et al.; U.S. Patent Application Serial No. 342,153, filed April 24, 1989, entitled "Method of Processing Siloxane-Polyimides for Electronic Packaging Applications" by H.S. Cole, et al.; U.S. Patent Application 289,944, filed December 27, 1988, entitled "Selective Electrolytic Deposition on Conductive and Non-Conductive Substrates" by Y.S. Liu, et al.; U.S. Patent Application Serial No. 312,536, filed February 17, 1989, entitled "Method of Bonding a Thermoset Film to a Thermoplastic Material to Form a Bondable Laminate" by R.J. Wojnarowski; U.S. Patent Application Serial No. 363,646, filed June 8, 1989, entitled "Integrated Circuit Packaging Configuration for Rapid Customized Design and Unique Test Capability" by C.W. Eichelberger, et al.; U.S. Patent Application Serial No. 07/459,844, filed January 2, 1990, entitled "Area-Selective Metallization Process" by H.S. Cole, et al.; U.S. Patent Application Serial No. 07/457,023, filed December 26, 1989, entitled "Locally Orientation Specific Routing System" by T.R. Haller, et al.; U.S. Patent Application Serial No. 456,421, filed December 26, 1989, entitled "Laser Ablatable Polymer Dielectrics and Methods" by H.S. Cole, et al.; U.S. Patent Application Serial No. 454,546, filed December 21, 1989, entitled "Hermetic High Density Interconnected Electronic System" by W.P. Komrumpf, et al.; U.S. Patent Application Serial No. 07/457,127, filed December 26, 1989, entitled "Enhanced Fluorescence Polymers and Interconnect Structures Using Them" by H.S. Cole, et al.; and U.S. Patent Application Serial No. 454,545, filed December 21, 1989, entitled "An Epoxy/Polyimide Copolymer Blend Dielectric and Layered Circuits Incorporating It" by C.W. Eichelberger, et al. Each of these Patents and Patent Applications is incorporated herein by reference.

This high density interconnect structure provides many advantages over prior art interconnection systems. In particular, it enables a very compact assembly of a multichip or multicomponent electronic system. This compact assembly minimizes the length of conductor runs which interconnect different chips and thus minimizes transit time delays between chips which can be an important factor in high speed systems. Further, unlike many prior art systems, this interconnection system facilitates high yield assembly of multichip circuits because the high density interconnect structure can be removed from a malfunctioning system without damage to good chips. After removal of the high density interconnect structure, faulty or marginal chips can be removed from the substrate and replaced with other chips. After replacement of any faulty chips, a new high density interconnect structure is formed on top of the chips and substrate. Alternatively, if the cause of the malfunction is in the high density interconnect structure itself, no chip removal and replacement needs to be done before fabricating a corrected interconnection structure. As a consequence of this reworkability, a production yield of essentially 100% is achieved by repairing any malfunctioning systems.

The above identified background high density interconnect structure patents and applications have focused, in their illustrative embodiments, on the interconnection of chips which are placed edge-to-edge for maximum density and then interconnected into digital computers and other systems. While not directly addressed in those background patents and patent applications, the illustrative embodiments therein assume that an overall system package or enclosure is large enough to enclose the high density interconnect structure. This assumption is clearly appropriate for such systems as digital computers, other electronic systems whose overall housing can be adapted to the high density interconnect structure's configuration. However, there are systems in which components that it might be desirable to interconnect using a high density interconnect structure must be placed directly adjacent to other portions of the system in a portion of a housing which either must have a predetermined configuration which is incompatible with a straightforward high density interconnection of the electronic components, or in which trade-offs are involved which make it desirable that

the high density interconnect structure be made even smaller than is achieved with a straightforward rectangular high density interconnect assembly in which external contact pads for connection to other parts of a system are provided on the upper surface of the ceramic substrate of the high density interconnect structure. Consequently, a modified high density interconnect structure providing greater flexibility for adjustment to overall package constraints is desirable.

Accordingly, a primary object of the present invention is to provide a high density interconnect structure in which the lateral area required by the high density interconnect structure can be reduced without adverse effect on the interconnection function.

The above and other objects which will become apparent from the specification as a whole, including the drawings, are achieved in accordance with the present invention by a high density interconnect structure in which the completed dielectric/conductor overlay structure includes a flexible portion which is not bonded to a rigid substrate or carrier. For added ruggedness, this flexible portion of the high density interconnect structure may include a support member which is bent in the process of bending the flexible portion of the high density interconnect structure out of the plane-of one portion of the system in a manner in which the conductors of the high density interconnect structure are held in compression (that is, disposed on the concave side of the bent support member) so as to prevent introduction of adverse, stress-induced effects or changes in the conductor structure as a result of bending the flexible portion of the high density interconnect structure.

Several different methods may be used to produce such a flexible high density interconnect structure. One method is to place the substrate containing the chips or other components to be interconnected in a temporary carrier or fixture which has a larger area than the final interconnect structure will have and which also contains an interconnect support layer which may be selectively removed from the high density interconnect structure after completion of the high density interconnect structure fabrication process. The high density interconnect structure dielectric/conductor overlay is then fabricated on top of the carrier, support member, substrate and chips. After completion of the fabrication of this high density interconnect structure, the chips, substrate, support member and the overlying portion of the high density interconnect structure may be removed, as a unit, from the carrier by appropriate means such as cutting the dielectric layers of the high density interconnect structure along the edge of the desired interconnect structure to allow removal of the completed desired structure from the carrier (the interconnect structure is preferably bonded to the carrier during fabrication for quality control reasons). Alternatively, the carrier could be removed by being dissolved in a solvent or etchant or by other means.

Thereafter, where an unsupported flexible portion of the high density interconnect structure is desired, the support member is selectively removed from that region to leave the dielectric/conductor overlay structure unsupported in that area. Alternatively, where the high density interconnect structure is to be bent upward away from the previous location of the carrier, the support member may be relatively thin and left in place and bent to hold the high density interconnect structure in a desired position with the high density interconnect conductors in compression because they are disposed on the inside of the curve created by bending the support member.

Where desired, the dielectric layer or layers of the high density interconnect structure may be removed to leave conductive tab extensions of the high density interconnect conductors for connection of the high-density-packaged system to external systems or components.

Where greater ruggedness of such conductive tabs is desired, those tabs may initially be part of a lead frame to which the dielectric of the high density interconnect structure are bonded and appropriate conductors of the high density interconnect structure are connected during the high density interconnection fabrication process. The individual tabs may be separated from each other following completion of the HDI fabrication process by severing a connecting portion of the lead frame. Under such circumstances, the high density interconnect structure dielectric layers are preferably left bonded to a portion of each of the conductive tabs to provide added support for the tabs. An edge connector card may also be used.

As an alternative to the use of a separate support layer to support the portion of the high density interconnect structure which will be rendered flexible at the end of the fabrication process, appropriate portions of the carrier or other support system may be left free of high density interconnect adhesive when laminating the initial dielectric layer of the high density interconnect structure to the chips and substrate, provided that an appropriate mechanism for removing heat from those portions of the dielectric during metal deposition by high energy processes such as sputtering. Glues and adhesives which are differentially dissolvable relative to the high density interconnect adhesive, vacuum hold-down and so forth may be used to provide sufficient dielectric/substrate thermal contact to provide this heat removal. This renders the final high density interconnect structure easily separable from those portions of the carrier or fixture. As a further alternative, release layers may be incorporated in the fabrication process in appropriate locations to allow subsequent separation of the high density interconnect structure from the carrier, substrate or other support structure as may be con-

sidered desirable.

Efficient cooling of the final system can be provided by removing all supporting structures after completion of fabrication and test to leave just electronic components bonded to the high density interconnect structure which may then be "rolled up" and placed in a coolant flow. The coolant may be freon in a gas expansion cooling system or a liquid or gas which remains in that state.

A "picture frame" portion of a support member may be retained on the high density interconnect dielectric to maintain dimensional stability in the dielectric area within the picture frame to hold contact pads within the high density structure in alignment for bonding to a separate structure by soldering, laser welding and so forth.

The invention, both as to organization and method of practice, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings in which:

Figure 1 illustrates a high density interconnected system including a flexible portion which allows the I/O lines of the interconnect structure to be bent out of the plane of the substrate;

Figure 2 illustrates a high density interconnected system which includes two substrates or modules, which in their final configuration, are disposed in non-parallel planes and interconnected by a bent, flexible portion of the high density interconnect structure;

Figures 3-7 illustrate successive steps in a process for fabrication of a high density interconnect structure which includes flexible portions;

Figures 8-10 illustrate some alternative manners of supporting the substrates and high density interconnect structure during the fabrication process in order to facilitate provision of a flexible high density interconnect structure;

Figure 11 illustrates an embodiment which includes metal foil, sheet or other rugged connection tabs which extend from the flexible high density interconnect structure at the end of the process;

Figures 12 and 13 illustrates two stages of a modified fabrication process which leads to the Figure 11 structure;

Figure 14 illustrates a substrate and an edge connector card ready for interconnection;

Figure 15 illustrates an array contact pad arrangement for connection of the completed flexible high density interconnect structure to an external portion of the system;

Figure 16 is a side view of the Figure 15 structure illustrating the alignment of the contact pads of its two parts;

Figure 17 illustrates a transfer the process for supporting the high density interconnect structure during selective or non-selective removal of a support member from that structure;

Figure 18 illustrates a flexible high density interconnect having the chips and other components bonded directly to it and free of substrates; and

Figure 19 illustrates the structure of Figure 18 "rolled up" and inserted in a coolant flow channel.

Figure 1 is a three-dimensional view of a system 10 comprised of a substrate 14 having a plurality of chips 20 mounted in a cavity or cavities therein and having a high density interconnect structure 30 in accordance with the , present invention bonded to the upper surface of the chips and substrate and providing electrical interconnections among the chips and to the outside world. Substrate 14 may preferably be alumina or another electrically insulating thermally conducting material whose thermal coefficient of expansion closely matches that of the chips 20. The high density interconnect structure 30 comprises a dielectric layer 32 which may preferably comprise a thermoset layer of polyimide which may preferably be KAPTON® polyimide available from E. I. DuPont de Nemours which is adhesively bonded by a thermoplastic adhesive to the upper surface of the chips, the substrate and a support member 16. The thermoplastic adhesive may preferably be a polyetherimide resin available from General Electric Company under the trade name ULTEM®.

The support members 16 may preferably be Kovar® or another low expansion coefficient metal whose thermal coefficient of expansion closely matches that of the alumina substrate 14. This is to facilitate manufacture of this interconnect structure by assuring that differences in thermal coefficients of expansion do not interfere with proper fabrication of the structure. Further, use of ferric chloride as an etchant to remove kovar is compatible with the rest of the high density interconnect structure materials and process steps. Kovar is readily available in 10-20 mil thicknesses which are thicker than necessary for this use and stiff enough that a thinner sheet or foil of kovar is desirable for bending.

A pattern of metal conductors 34 is disposed on the upper surface of the dielectric layer 32 and makes contact to various contact pads (only one shown) of the chips 20 through via holes (only one shown) in the dielectric layer 32. It will be noted, that this interconnection structure includes unique features when fabricated by first forming the dielectric layer on the underlying structure, then forming the via holes by "drilling" from above in the dielectric layer and then depositing the metal of the conductors 34. In particular, the external configuration of the metal in the via hole takes on the shape of the via hole, rather than vice versa as would be the case if the metal in the via hole were formed first and the dielectric filled in around it. This typically results in a via hole which is wider at the top than at the bottom because of the nat-

ure of the laser drilling process. This also provides improved metal continuity between the rest of a conductor and the portion of it which is disposed in the via hole, since the via hole surface on which the metal in the via hole is deposited has a sloping-upward-and-outward configuration which is known from the semiconductor arts to provide a deposited metallization layer with better step coverage than is provided by a vertical wall. Further, when made in the preferred manner described in the background Patents and Patent Applications, the metal conductor's upper surface has a depression or dimple in it over the via hole because the metal is deposited to a substantially uniform thickness rather than up to a particular plane. The conductors 34 are shown cut-away and omitted (except for one) over the substrate 14 for drawing clarity and because the connection of high density interconnection conductors to the chips and substrates is the subject of earlier patents and applications which are listed above and which fully describe the resulting structure and the process of making it. A second dielectric layer 36 is disposed over conductors 34 and dielectric layer 32. These structures are well described and illustrated in background HDI U.S. Patent 4.783,695 as well as others. The portion 38 of the interconnect structure which is disposed on substrate 14 and chips 20 is a rigid structure which is firmly adhered to the substrate and chips. To the left and right of the substrate 14 in Figure 1, the interconnect structure portions 39 are flexible. As illustrated at the right-hand side of the figure, the support member 16 and the associated portion of the interconnect structure are bent upward relative to the plane of the substrate in a smooth curve to place the conductive lines 34 perpendicular to the plane of the upper surface of the substrate 14. At the upper end of this bent structure in the figure, conductive tabs 35, which are continuous with the conductors 34 within the dielectric structure, protrude beyond the dielectric structure. The tabs 35 may comprise the same conductor arterial in the same cross-sectional configuration as the conductors 34. In that event, these exposed tabs are initially formed as parts of the conductive runs 34 and made protruding by selectively removing the dielectric of the interconnect structure adjacent to those tabs. This removal may be done by laser ablation, by immersion of that portion of the interconnect structure in a solvent for the dielectric material (if there is such a solvent) or by other means appropriate to the particular materials used in fabricating the structure. Similar conductive tabs 35 extend beyond the dielectric at the left-hand end of the figure.

When the support member 16 is bent from a planar configuration into the configuration illustrated in Figure 1, it places the conductive lines 34 of the interconnect structure in compression because the interconnect structure is on the concave side of the support member 16 (this is referred to as an inside bend) and because the interconnect structure (dielectric and conductors) is more elastic than the support member. This is desirable since it ensures that the lines 34 will not fracture due to stresses. While in a typical application of such a flexible interconnect structure, the tabs 35 at the left-hand side of the figure would normally be either in the plane of the substrate or bent in the same direction as the portion of the structure to the right of the substrate, this structure may be bent downward relative to the substrate. The support member 16 should be omitted at such a bend in the interconnect structure, since otherwise, the interconnect conductors 34 would lie on the convex side of the support member (this is referred to as an outside bend) and would be placed in tension because the interconnect structure (dielectric and conductors) is more elastic than the support member. Such a configuration is considered undesirable because of the risk of stress-induced failures in the relatively thin conductors 34 despite the fact that they are preferably made of highly ductile copper. The support layer can be retained in an outside bend without risk or with reduced risk by thinning the support member in a uniform manner, by using a very thin support member to begin with (preferably about 3 to 5 mils thick, or by selectively removing the support member to leave a thick "picture frame" of the support member along the edges of the structure where no conductors are and across the ends of the bend to hold the sides of the frame in position. If desired, a second layer of conductors could be disposed on dielectric layer 36 and, if desired, a third dielectric layer could be disposed over those conductors.

A further embodiment 10' of the invention is illustrated in a three dimensional view in Figure 2. This structure is similar to the Figure 1 structure 10 with the exception that the system employs two separate substrates 14 or modules which are spaced apart by a flexible portion 39 of the interconnect structure which is bent to place the two substrates 14 in perpendicular planes. In this specification reference numerals which are the same in different figures identify similar elements which serve similar functions. Often these elements are discussed only with respect to the first figure in which they appear. A reference numeral to which a prime ('), a double prime (") or an asterisk is suffixed identifies a modified element which serves a similar function to the element identified by the plain reference numeral

As illustrated in Figures 1 and 2, the interconnect structure comprises two dielectric layers and a single metal interconnect layer. Alternatively, a single dielectric layer (32) could be used or two conductive layers in combination with two or three dielectric layers and two conductive layers could be used.

Use of the flexible HDI interconnect structure carries with it a potential disadvantage that the overall high density interconnect system is physically larger

than it might be if fabricated in a strictly rigid configuration. Consequently, propagation delays will be increased by the increased lengths of the interconnecting conductors. However, there are many systems in which propagation delays in the external leads of the high density interconnect system are not as crucial to overall system operation as electrical delays between the various components which are connected on the substrate 14 by the high density interconnect structure. Consequently, in many systems, the flexible high density interconnect structure will provide substantial packaging and/or system advantages without introducing any significant system detriments.

A method of fabricating this high density interconnect structure will now be described. In Figure 3, the components of the system 10 are illustrated ready for the fabrication of the high density interconnect structure. In particular, the substrate 14 and the support members 16 are disposed in a carrier 12 in depressions or cavities whose depths are selected to place the upper surface of the support members 16 in the same plane as the adjacent portion of the upper surface of the carrier 12 and the upper surface of the substrate 14. Within the substrate 14, the chips 20 are placed in appropriate cavities 15 which place their upper surfaces in that same common plane. This coplanar alignment of the upper surfaces of the various portions of the structure is to facilitate fabrication of the high density interconnect structure as is explained in some of the background patents and applications.

In Figure 4, a completed high density interconnect overlay structure 30 is illustrated overlying the carrier 12, the substrate 14, the support members 16 and the chips 20. Depending on the complexity of the system and the particular application, additional dielectric layers and interconnecting conductor layers may be provided in the manner taught in the background patents. The detailed process for fabricating this structure has been explained briefly in the Background Information portion of this specification and is explained in much more detail in the background high density interconnect U.S. Patents and Patent Applications cited above.

At the stage illustrated in Figure 4, the process of fabricating this high density interconnect structure 30, which is described in the background patents and applications, is complete in the sense that all of the interconnections and dielectric layers are present. At this stage of the process, the interconnect structure is ready for removal from the carrier 12. This may be done by cutting the high density interconnect structure along the boundary between the upper surface of the carrier 12 and the support members 16 and the substrate 14. This cutting may be done with a knife or other sharp object or by laser cutting. It is preferred to have all of the interconnection conductors 34 spaced from this cut line in order to assure that no damage to the conductors will occur during this cutting process. Since any conductors 34 crossing this cut line would be cut anyway, there is normally no need for such conductors to cross these cut lines. After structure 30 is cut and the system is removed from the carrier 12, the high density interconnect structure appears as illustrated in Figure 5.

If desired, the conductors 34 may cross the cut line to connect the "final" structure to temporary test structures and contact pads for connection to test systems to facilitate testing of the complete interconnected system prior to cutting of interconnect structure at the cut line. Use of such a testing structure facilitates repair of the system in the simplest manner in the event that reworking of the system should be necessary, since the-various components are still mounted in the carrier at this stage of the process.

At this stage, the left-hand and right-hand wings or extensions of the high density interconnect structure beyond substrate 14 (which are bonded to the support members 16), are flexible in the sense that they can be bent upward in the figure without damage to the structure, provided the support members 16 are appropriately thin. Where it is desired to provide greater flexibility or to be able to bend the interconnect structure in the opposite direction without risk to the conductors, appropriate portions of the support members 16 may be selectively thinned in a uniform or patterned manner or may be completely removes, as may be preferable in the particular application. This removal or thinning may preferably be done by ferric chloride spray etching in the case where the support members are Kovar®. The structure shown in Figure 6 has the support member 16 selectively removed from both the left-hand end and right-hand end of the structure. It will be understood that support member 16 may alternatively be completely removed or not removed at all.

In order to provide tabs for bonding the interconnect structure to a larger system, it may be considered desirable to provide exposed conductive tabs 35 at the end of the structure as illustrated in Figure 7. Where this is considered desirable, the dielectric layer of the interconnect structure may be removed by laser ablation, by being dissolved in a solvent (if one is available by the dielectrics used) or by other means as may be appropriate to the particular materials of which the system is fabricated. Where the dielectric layer includes a thermoset polyimide material, solvent dissolving of the dielectric is not generally feasible with the result that user ablation or other appropriate techniques should be used. Since the tabs 35 are merely portions of the high density interconnect metal which extend beyond the dielectric, they are extremely fragile due to the typical dimensions for such conductors of from 2 to 20 mils wide by from 2 to 10 microns thick. Consequently, appropriate care must be used in forming, handling and bonding these tabs. While the tabs 35 are shown disposed at the end of

the high density interconnect structure, it should be understood, that if desired, the conductors 34 could be exposed at an intermediate location instead of or in addition to at the end of the high density interconnect structure.

Figures 8-10 illustrate alternative means to the Figures 3-7 means of rendering the to-be-flexible portions of the high density interconnect structure removable from the carrier. In particular, in Figure 8, mosaic blocks or support members 16' are provided in the cavity in the carrier 12' between the substrates 14 and the edges of the cavity and between adjacent substrates. In laminating the first layer of dielectric 32 to this carrier and the substrates, the high density interconnect adhesive is omitted from the mosaic blocks 16' so that the lamination process does not bond the dielectric to these portions of the structure. While it would be desirable to leave these portions of the structure completely unbonded to facilitate subsequent removal of the completed structure from the carrier, process and material limitations normally prevent this from being done. In the presently preferred method of fabrication, the initial metal adhesion promotion layer is applied to the KAPTON® polyimide layer by sputtering. This is a high energy process which transfers on the order of 10 watts of energy to the KAPTON per square inch. This tends to heat the film causing outgasing, dimensional distortion and adhesion poisoning which prevent good metal adhesion. With the film bonded everywhere, the substrate, chips, support members and carrier provide a sufficiently effective heat sink to carry this heat away without significant detrimental effects. This is true even where a 40-50 mil span of the KAPTON is left unsupported or unbonded. However, an unbonded span of 100 mils yields marginal characteristics and longer spans become unusable. Several effects are involved in this. First, without adequate heat sinking, the applied energy heats the KAPTON film which leads to thermal distortion of the film in the form of crinkling, warpage and so forth. Further, this thermal distortion also prevents metal adhesion with the result that the metal will not stay in place. In marginal situations, poor metal adhesion can result even if crinkling and warpage are not apparent. For this reason, if sputtering or other high energy processes are used to deposit even the first layer of metal on the KAPTON film, the film must be adhered to some form of heat sink during the metal deposition process. Techniques which may be used include using a different glue or adhesive on the mosaic blocks 16' to sufficiently adhere the film for heat sinking purposes while making them removable by dissolving in a solvent which is inert to the desired portions of the high density interconnection structure. Subsequent dissolving of the alternative adhesive can be facilitated by making the carrier 12 porous or providing it with access holes through which the solvent for the adhesive can be provided directly to the adhesive during the high density interconnect/carrier separation process. Vacuum hold-down can be used if sufficient thermal contact can be achieved despite the vacuum environment in which the sputtering process takes place. Alternatively, if the metal is deposited by a lower energy process which does not cause an undesirable increase in thermal energy in the KAPTON, then, these regions may be left unbonded. Such alternative processes can include sputtering of thinner layers or at a slower rate. Thus, where a thin titanium layer is deposited directly on the Kapton for adhesion promotion and a layer of copper is deposited thereon, less heating results when that copper layer is only made thick enough to ensure complete coverage of the titanium (to prevent the formation of titanium oxide when the part is removed from the sputtering chamber), unbonded segments of Kapton may be as long as about 200 to 250 mils. Another alternative process is electroless deposition of the metal, although choosing electroless deposition as the metal deposition technique may undesiraly limit the metals which can be used.

Following completion of the fabrication of the high density interconnect structure, the interconnect structure, including the substrate and chips, may be cut from the carrier 12' near the left-hand end of the carrier at the gap between the mosaic block 16' and the ledge of the carrier and near the right-hand end of the carrier between the block 16' and the ledge or lip of the carrier. Thereafter, when the high density interconnect structure is removed, the blocks 16' remain behind, leaving fully flexible portions of the high density interconnect structure at those locations.

Alternatively, as illustrated in Figure 9, the support blocks 16' may be omitted and replaced by portions of the carrier 12" itself which are kept adhesive free or differentially bonded as discussed above. In this case, the cutting is done at the edge of the adhesive bonded portions of the high density interconnect structure nearest the ends of the carrier. These adhesive free portions may be provided by use of a mask during adhesive deposition.

As illustrated in Figure 10, adhesive may be applied to the entire structure and a release layer which does not bond to the adhesive or a pair of superimposed release layers 17 which do bond to the adhesive, may be placed in the locations where the flexible-interconnect structure is desired. While in the illustrated cross-section the release sheets appear to be three laterally spaced-apart pieces, it will be understood that, in fact, they are preferably continuous stencils or templates having holes therein in the locations where adhesion of the high density interconnect structure is desired. Thus, the release layers in this embodiment are in the form of a rectangular figure "8", assuming the structure is only one substrate wide in the direction perpendicular to the paper (it could be two or more substrates wide in that direction, if des-

ired). A suitable material for such a release layer is DuPont's PFA Teflon, although many other dielectric or conductive materials can be used. The overlying dielectric layer 32 is then laminated to this structure and the fabrication of the high density interconnect structure proceeds as previously described.

One concern with respect to the connection tabs 35 as described above, is that they can be extremely fragile due to the manner of their production as part of the built-up interconnect-structure conductors which are not normally made so thick as to be highly durable in such an exposed application. As an alternative to the use of such extensions as the external connection tabs, lead frame tabs 35' may be included in the structure as shown in Figure 11. In Figure 11, the connection tabs 35' which extend from the high density interconnect structure are substantially thicker than conductor runs within the high density interconnect structure and are connected to the conductors within the high density interconnect structure in the same manner as other connections (through via holes in intervening dielectric material).

In Figure 13 a comb-like lead frame 31 is intermessed with a comb-like support member 16 to provide a substantially planar surface to which the dielectric layer 32 is bonded.. The lead frame 31 comprises a plurality of connection tabs 35' and a connecting member 31C which holds the connection tabs in fixed relative locations during the fabrication process. The lead frame 31 is placed in the same carrier cavity as the support member 16. Alternatively, the support member 16 may be a part of the lead frame (with the individual tabs 35' being separated form the rest of the support member, except at their connection to the connecting portion 31C) or the tabs may be isolated by selective removal of the support member after the completion of the fabrication process.

The dielectric layer 32 is then bonded to the structure. Thereafter, via holes are formed in dielectric layer 32 and the connecting metal runs formed on top of that dielectric layer and extending into those via holes.

This leaves tabs 35' exposed on the underside of the dielectric of the interconnect structure at the end of the fabrication process.

During the fabrication process, the appropriate ones of the interconnection conductors of the high density interconnect structure are formed in ohmic contact with appropriate ones of the tab leads 35'. Following removal of this completed high density interconnect structure from the carrier 12, the connecting portion 31C of the lead frame is severed from the high density interconnect structure to leave physically separate conductive tabs 35'. Thereafter, the dielectric, which covers the to-be-exposed portions of the tabs 35' is selectively removed to expose those portions of the tabs.

As a further alternative for providing connection tabs, an edge connector "card" or another preformed connector module may be flexibly or rigidly connected to an HDI interconnect structure as may be appropriate to an overall system package. In Figure 14, a portion of a modified carrier 12* is illustrated having a substrate 14 disposed therein along with support members 16 and an edge connector card 18 which are ready for fabrication of a high density interconnect structure thereon which will interconnect the chips 20 of the substrate 14 and the edge connector contacts 19 of the edge connector card 18. As illustrated, the edge connector card 18 has electrically separate contacts disposed on opposite sides of the card, but aligned with each other. The electrically separate contacts on the lower side of the card in the figure are brought to the upper surface through eyelets, rivets, plated through,,or filled holes, etc. 19A for connection to the high density interconnect structure conductors in a substantially planar manner as has been described. It will be understood that following fabrication of the high density interconnect structure, the entire system, including the substrate 14 and the edge connector card 18, is removed from the carrier as a unit in a manner similar to those in which earlier described embodiments are removed from their carriers. After completion of the fabrication of the high density interconnect structure, the high density interconnect dielectric can be removed from the edge connector contacts 19 in a manner similar to that inwhich the dielectric is removed from the connection tabs 35, such as by laser ablation, or in this case by including release layers over the ends of the contacts as part of the fabrication process. The flexible portion of the high density interconnect structure which is, at least during fabrication, disposed on the support member 16 serves to flexibly connect the edge connector card to the high density interconnect structure substrate 14 with the result that the edge connector card may be positioned in any of a variety of desirable orientations relative to the substrate 14. Instead of a double-sided edge connector card, a single sided edge connector card could be used. In that situation, it is considered preferable to orient the card with its contact side up in the figure so that there is no need bring lowerside contacts to the upper surface for connection to the high density interconnect structure conductors. Alternatively, the edge connector card can be a printed circuit board which includes other components in addition to an edge connector. As a further alternative, the edge connector contacts can be formed as part of the high density interconnect structure fabrication process.

In Figures 15 and 16 an alternative configuration for connecting a flexible high density interconnect structure to an external portion of a system is illustrated. The illustrated portion of the flexible high density interconnect structure includes a picture or support frame 62 which is bonded to the dielectric of the high density interconnect structure 30. The frame

62 is the remaining portion of a support member 16 from which the interior portion of the support member has been selectively removed. Thus, the structure illustrated in Figure 15 is inverted relative to the other illustrations in the sense that the support member side of the structure is illustrated as being upward in the figure. As may be seen more clearly in Figure 16, the contact pads 37 are exposed at the lower surface of the interconnect structure 30 and have been configured and positioned for direct alignment with contact pads 77 on an external portion 70 of the system to which this flexible high density interconnect structure is to be connected. Removal of the central portion of the support member to leave the picture frame 62 enables the contact pads 37 of the high density interconnect structure to be visually aligned with the contact pads 77 of the external portion 70 of the system. The picture frame 62 itself is retained in order to maintain the high density interconnect structure 30 in proper tension so that its dimensional stability remains intact during the process of aligning and bonding the pads 37 to the corresponding pads 77. Any of a wide variety of bonding processes may be used to bond the pads 37 to the pad 77. These include solder bump bonding and the use of thermal reflow to create the bond between the pads 37 and the pads 77, the use of conductive adhesives and the use of laser welding, among others. The conductors 34 which connect to the contact pads 37, are illustrated as single lines for drawing clarity and because depending on the size and spacing among the pads 77, the pads 37 may be substantially wider than the conductor lines 34.

Where a large number of closely spaced small contact pads 37 are required, the conductors 34 may be disposed in a variety of layers in the high density interconnect structure in order to fit the required number of conductors 34 into the space available between rows of the contact pads 37.

Following bonding of the pads 37 to the pads 77, the picture frame portion 62 of the support member may be left in place or may be removed as by ferric chloride etching in the case of Kovar as may be considered desirable for the particular system.

If it is desired to retain the frame 62 as a permanent part of the system, but presence of conductive material in that location is undesirable, then the frame may be prefabricated out of dielectric material and provided with a support member 16 within its opening during the fabrication process. That support member is then removed after completion of the high density interconnect structure fabrication process. In such circumstances, the frame may be ceramic or any other appropriate dielectric material. Prefabrication of the frame is unnecessary when a dielectric which can be selectively removed is used to form the frame.

In Figure 17, a process for selectively removing the support members 16 is illustrated. In Figure 17, the interconnected system, including the substrate 14, the support member 16 and the interconnect structure itself has been bonded by an adhesive 52 at the upper surface of the interconnect structure to a block 50. This secures the interconnect structure in an easily handled, well-supported manner. The support members 16 may then be masked in a desired pattern (if selective removal of the support members is desired) and the exposed portions of those supports removed by spray etching. Where those support members are Kovar, ferric chloride is a preferred spray etchant. This high density interconnected structure may be left mounted on the block 50, if desired, or may be subsequently separated therefrom by dissolving the adhesive 52 which bonds the interconnect structure to the block in an appropriate solvent, by dissolving the block itself or by heating the structure to a temperature at witch the adhesive 52 becomes sufficiently fluid that the interconnect structure may be easily slipped laterally off the block 50.

Figure 18 illustrates an array of electronic components or chips 20 interconnected by a high density interconnect structure 30 which has been rendered flexible by removal not only of the carrier and any support members, but also by removal of the substrates 14 to leave just the electrical components connected by the high density interconnect structure 80. That is, the electronic components are free of external substrates. This structure may be advantageously used where space requirements are particularly tight with the result that even the substrate thickness creates problems and where the flexible interconnect structure must fit into a closely defined configuration which the presence of the substrate would prevent. While a two dimensional array of chips is shown in Figure 18, it will be understood that this is also applicable to linear arrays.

Another reason for removing the substrates can be in order to maximize thermal transfer in a structure such as that shown in Figure 19. In Figure 19, the system 80 has been "rolled up" to form a small, relatively compact spiral or cylinder and has been installed in a tubular housing 84 with an end of the interconnect structure extending through a sealing slot 85. The chips 20 and the portion of the structure 80 within the conduit 84 are disposed in a sealed coolant conduit through which a coolant, indicated by the arrows 86, is pumped in order to provide maximum cooling of the individual chips. The coolant 86 may be a liquid such as water, or a gas ,such as nitrogen, or a refrigerant (such as freon) of the type used in compressor driven cooling systems which rely on expansion of liquid to gas for cooling. Where the coolant 86 is such a refrigerant, it may be in either a liquid or a gaseous state at the time it enters the conduit 84 and begins passing the system 80. Depending on the flow rate of the coolant and the power dissipation and size of the system, coolant may emerge from the system 80 still in a liquid form, in a gaseous form or as a mixture thereof. This

system configuration provides the ultimate in cooling by exposing the chips 20 directly to the coolant without any thermal interfaces therebetween.

While not shown in Figure 19, a structure may preferably be provided to hold the various turns of the rolled up system 80 in fixed relation to each other. One appropriate structure for this purpose is a modified photographic film development film holder of the type used to hold an individual roll of film for development in a cylindrical-can film development system. That is, in which the edges of the film are held in spiral tracks in two circular caps which are mostly open space in order to facilitate the flow of film development chemicals therethrough. In the cooling environment, naturally, the openings in that modified rack are for the flow of the coolant rather than film development chemicals. Many other support techniques may also be used.

In Figure 19, the system 80 is shown rolled with the chips 20 disposed on the outside of the roll, it will be recognized that the system can be rolled in the opposite sense so that the chips are disposed on the inward side of the dielectric layer of the system, as rolled. The system 80 may alternatively be left flat, folded or otherwise manipulated prior to insertion into an appropriate cooling chamber, or may be left unenclosed, if desired.

There has been described in the foregoing, high density interconnect structures with a flexible portion suitable for enabling relative movement between different portions of an electronic system interconnected by that structure. Different components of the system are disposed in different, non-parallel planes, in a rugged, flexible, high density interconnect structure which can be assembled in a reliable, high yield manner.

In each of the illustrative embodiments, a linearly arranged system is illustrated in which flexible portions of the interconnection structure extend only from two opposed ends of the chip containing substrate in the completed system. However, such flexible portions can extend in any desired direction, including four mutually perpendicular directions or at any other desired directions, as may be appropriate for a particular system being fabricated.

In each of the illustrative embodiments, the flexible portion of the high density interconnect structure has initially been formed over the carrier, rather than on the substrate in which chips are disposed, however, it should be understood that in a situation where it is considered desirable to have a flexible end to the interconnect structure itself, but the substrate length does not need to be overly restricted, the to-be-flexible portion of the high density interconnect structure can be fabricated directly over the substrate itself. In that situation, use of a release layer may be preferable to use of a support member to which the high density interconnect structure is bonded.

While the invention has been described in detail herein in accord with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art.

Claims

1. An electronic system including a flexible interconnection structure comprising:
   a flexible interconnection comprising:
   a layer of flexible dielectric material, and
   a plurality of flexible conductors supported by said dielectric layer, and
   an electronic component having a major surface having contact pads disposed thereon, said electronic component having said major surface thereof bonded to said dielectric of said flexible interconnect structure and having selected ones of said contact pads connected to selected ones of said flexible conductors.

2. The electronic system recited in claim 1 wherein:
   said contact pads are connected to said flexible conductors by conductive material disposed in via holes in said dielectric material.

3. The electronic system recited in claim 1 wherein:
   at least some of said flexible conductors are embedded in said dielectric.

4. The electronic system recited in claim 1 wherein:
   the flexible portion of said interconnection structure includes a support member bonded to the dielectric of said structure.

5. The electronic system recited in claim 4 wherein:
   said support member is curved toward said dielectric layer to hold said flexible conductors in compression in a location where said flexible interconnection structure is curved.

6. The electronic system recited in claim 5 further comprising:
   a second support member bonded to the other side of said flexible interconnect structure.

7. The electronic system recited in claim 6 wherein:
   said second support member is curved toward said dielectric layer to hold said flexible conductors in compression in a location where said flexible interconnection structure is curved.

8. The electronic system recited in claim 1 further comprising a substrate, and wherein:
   said electronic component is bonded to said substrate; and
   said dielectric is bonded to said substrate.

9. The electronic system recited in claim 1 wherein:
a plurality of said flexible conductors include a segment which is free of said dielectric material.

10. The electronic system recited in claim 9 wherein:
said dielectric-free segment is disposed at an end of said flexible interconnection structure to provide connections tabs for connection to external circuitry.

11. The electronic system recited in claim 1 wherein:
said flexible interconnection includes conductive connection tabs which extend from an end thereof.

12. The electronic system recited in claim 11 wherein:
said conductive connection tabs are connected to said flexible conductors through conductive material disposed in via holes in said dielectric material.

13. The Electronic system recited in claim 11 wherein:
said conductive connection tabs are integral with said flexible conductors.

14. The electronic system recited in claim 1 wherein:
said system includes an edge connector connected to said electronic component by said flexible interconnection.

15. A high density interconnect structure including:
a flexible interconnect structure comprising:
a layer of dielectric material,
a plurality of conductors disposed on said layer of dielectric material;
an array of contact pads disposed on a surface of said flexible interconnect structure;
a frame bonded to said flexible interconnect structure, said frame having an opening therein which encompasses at least a portion of said array of said contact pads.

16. The high density interconnect structure recited in claim 15 wherein:
said frame comprises metal.

17. The high density interconnect structure recited in claim 15 wherein:
said frame is metal.

18. The high density interconnect structure recited in claim 15 wherein:
said frame comprises dielectric material.

19. The high density interconnect structure recited in claim 18 wherein:
said frame comprises ceramic.

20. The high density interconnect structure recited in claim 15 wherein:
said frame and said array of contact pads are disposed on the opposite sides of said flexible interconnect structure.

21. The high density interconnect structure recited in claim 15 wherein:
at least some of said contact pads of said array are aligned with and bonded to contact pads on a structure external to said high density interconnect structure.

22. The high density interconnect structure recited in claim 21 wherein:
said contact pads of said array are bonded to said contact pads of said external structure by solder.

23. The high density interconnect structure recited in claim 21 wherein:
said contact pads of said array are bonded to said contact pads of said external structure by a weld.

24. The high density interconnect structure recited in claim 21 wherein:
said frame and said array of contact pads are disposed on the opposite sides of said flexible interconnect structure.

25. A high density interconnect structure comprising:
a plurality of electronic components;
a flexible interconnect structure comprising:
at least one dielectric layer, and
at least one patterned conductor layer,
the conductors of said patterned layer interconnecting said electronic components; and
at least some of said electronic components being free of external substrates.

26. The high density interconnect structure recited in claim 25 wherein:
at least a portion of said flexible interconnect structure is disposed in a spiral, whereby said electronic components are disposed in different planes.

27. The high density interconnect structure recited in claim 26 wherein:
said spiral is disposed in an external hous-

ing.

28. The high density interconnect structure recited in claim 27 wherein:

said external housing comprises a cooling conduit.

29. The high density interconnect structure recited in claim 25 wherein:

said electronic components are disposed in a coolant containing housing.

30. In a method of fabricating a high density interconnect structure of the type comprising a substrate having an electronic component disposed thereon, said component including contact pads thereon, said high density interconnect structure including one or more polymer dielectric layers disposed over said component and having apertures therein, one or more patterned conductive layers overlying selected ones of said dielectric layers and extending into selected ones of said apertures into ohmic contact with selected contact pads or other conductive layers, the method being one in which the electronic component is mounted on a substrate and the dielectric and conductor layers are applied thereto, the improvement comprising the step of:

rendering a portion of said high density interconnect structure flexible by separating it from said substrate.

31. The improvement recited in claim 30 wherein the step of rendering comprises the steps of:

including as part of said substrate a temporary support member for supporting said portion of said high density interconnect structure during said fabrication process; and

subsequently separating said temporary support member from the remainder of said substrate to render said portion of said high density interconnect structure flexible.

32. The improvement recited in claim 31 further comprising:

selectively removing said temporary support member from said high density interconnect structure.

33. The improvement recited in claim 31 further comprising:

removing said temporary support member from said high density interconnect structure.

34. The improvement recited in claim 30 in which said method includes adhesive bonding the first of said dielectric layers to said substrate and said component with a first, high density interconnect adhesive and wherein said improvement further comprises:

leaving a portion of said substrate free of said first adhesive whereby the portion of said interconnect structure disposed thereon is not bonded to said substrate by said first adhesive; and

the step of rendering comprises, after completion of the fabrication of said interconnect structure, separating said interconnect structure from said portion of said substrate to which is free of said first adhesive to render that portion of said interconnect structure flexible.

35. The method recited in claim 34 further comprising the step of:

providing a second adhesive on the portion of said substrate which is free of said first adhesive and over which said portion of said high density interconnect structure will be disposed.

36. The improvement recited in claim 30 in which said method includes adhesive bonding the first of said dielectric layers to said substrate and said component and wherein said improvement further comprises:

including a release layer in said interconnect structure for facilitating removal of a to-be-flexible portion of the completed interconnect structure from said substrate to render that portion of said interconnect structure flexible.

37. The improvement recited in claim 30 in which said method includes adhesive bonding the first of said dielectric layers to said substrate and said component and wherein said improvement further comprises:

providing a temporary support member which extends beyond said substrate and on which said portion is disposed; and

the step of rendering comprises subsequently separating said temporary support member from said substrate to render said portion of said interconnect structure flexible.

38. The improvement recited in claim 30 further comprising the steps of:

removing the dielectric material of said high density interconnect structure from all sides of a portion of a conductor in said flexible portion of said high density interconnect structure.

39. The improvement recited in claim 30 further comprising the steps of:

removing the dielectric material of said high density interconnect structure from all sides of a portion of each of a plurality of conductors in said flexible portion of said high density intercon-

nect structure.

40. The improvement recited in claim 30 further comprising the step of:
providing a connection tab extending from an end of said interconnect structure.

41. The improvement recited in claim 40 wherein the step of providing a connection tab comprises the step of:
removing the interconnect structure dielectric material from a portion of a conductor of said interconnect structure.

42. The improvement recited in claim 40 wherein the step of providing a connection tab comprises:
providing a plurality of connection tabs and the steps of:
including a preformed lead frame in said interconnect structure during the fabrication process; and
severing a connecting portion of said lead frame to provide separate connection tabs.

43. The improvement recited in claim 42 further comprising the step of:
removing the interconnect structure dielectric material from a portion of a first one of said connection tabs.

44. The improvement recited in claim 40 wherein the step of providing a connection tab comprises providing a plurality of connection tabs and the improvement further comprises:
providing said high density interconnect structure with an edge connector by bonding appropriate ones of said connection tabs to an edge connector.

45. The improvement recited in claim 30 further comprising the step of:
providing an edge connector at an end of said interconnect structure.

46. The improvement recited in claim 40 further comprising:
including as a part of said substrate a conductive lead frame including connection tabs and a connecting portion which connects said connection tabs, said connection tabs being held in fixed relation to each other;
during said fabrication process:
bonding the dielectric/conductor overlay interconnection structure to said lead frame,
connecting selected ones of said conductors of said interconnect structure to selected portions of said lead frame ; and
after completion of the fabrication of the interconnect structure severing the connecting portion of said lead frame to provide said interconnect structure with electrically separate connection tabs.

47. The improvement recited in claim 46 wherein:
said selected ones of said interconnect structure conductors are connected to said tabs through via holes in the dielectric of said dielectric/conductor overlay interconnection structure.

48. The improvement recited in claim 30 further comprising the step of:
providing an edge connector at an end of said interconnect structure.

49. The improvement recited in claim 48 wherein said step of providing an edge connector comprises the step of:
including a preformed edge connector in said assembly during the fabrication process.

50. The improvement recited in claim 48 wherein said step of providing an edge connector comprises the step of:
fabricating an edge connector as part of the fabrication process.

51. The improvement recited in claim 48 wherein said step of providing an edge connector comprises the step of:
bonding a preformed edge connector to said interconnect structure after completion of the process of fabricating the high density interconnect structure.

52. The method recited in claim 32 further comprising the step of:
selectively removing an interior portion of said support member to leave a picture frame surrounding a portion of said high density interconnect structure.

53. The method recited in claim 52 wherein a contact pad is disposed in alignment with the opening in said picture frame.

54. The method recited in claim 53 further comprising aligning said contact pad with a contact pad of an external structure and bonding said contact pads to each other.

55. The method recited in claim 54 further comprising the step of:
removing additional support member material following said bonding.

56. The method recited in claim 30 including the step of:

removing said interconnect structure and said chips from said substrate.

57. The method recited in claim 56 further comprising the step of:

rolling up said high density interconnect structure.

58. The method recited in claim 57 further comprising the step of:

inserting said rolled up high density interconnect structure in a housing.

59. The method recited in claim 58 further comprising the step of:

connecting said housing to a source of coolant.

60. A method of operating an electronic system of the type comprising a plurality of electronic components interconnected by a flexible high density interconnect structure comprising:

inserting said components and at least the portion of said flexible high density interconnect structure to which they are connected in a housing; and

flowing a fluid through said housing while said system is operating.

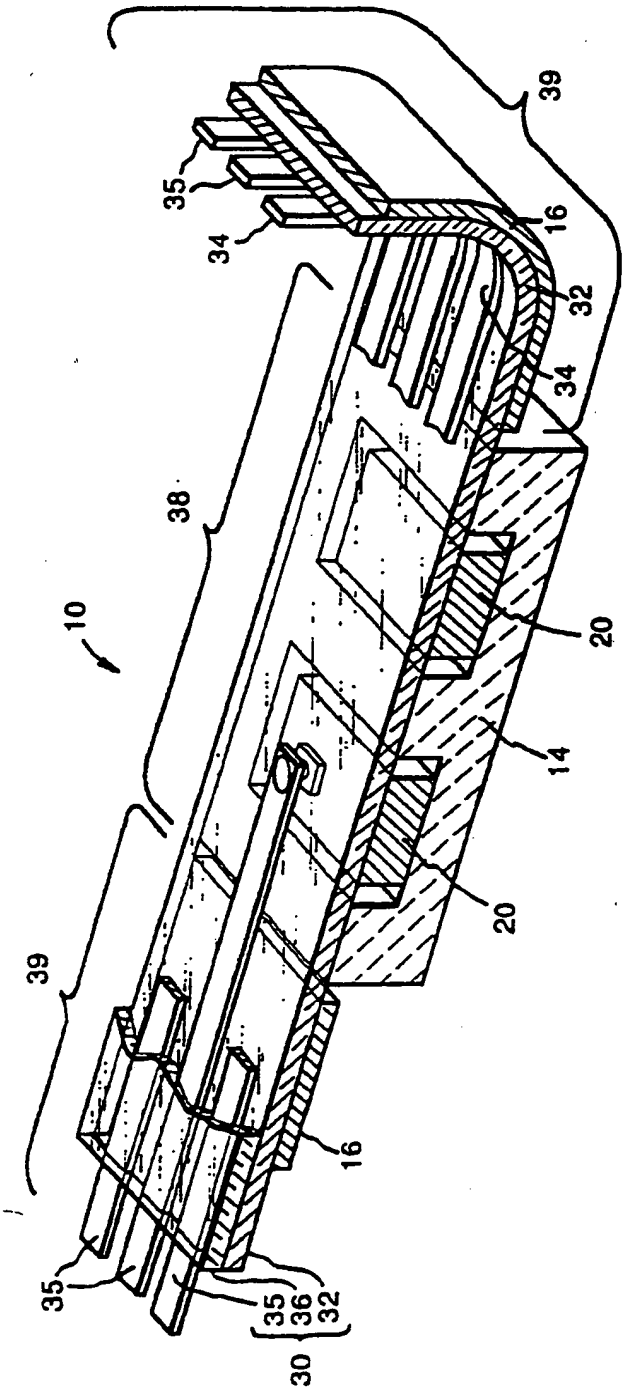
61. The method recited in claim 60 wherein the step of flowing comprises:

flowing a coolant through said housing to carry away heat which is generated by said components during operation of said system.

62. The method recited in claim 60 further comprising, prior to performing the step of inserting, performing the step of:

manipulating said flexible high density interconnect structure to place said electronic components in a compact volume configured to fit in said housing.

FIG. 1



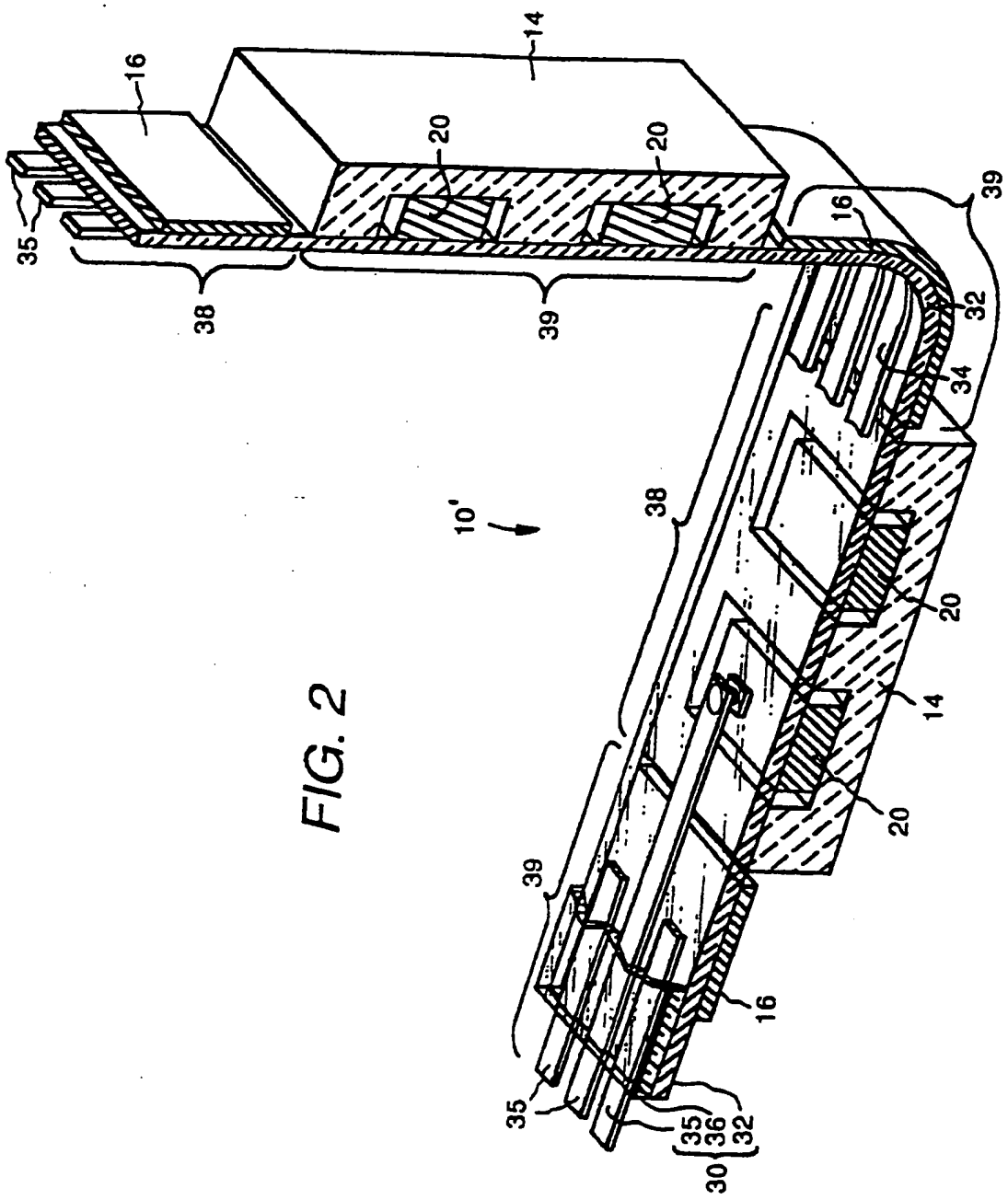


FIG. 2

FIG. 3

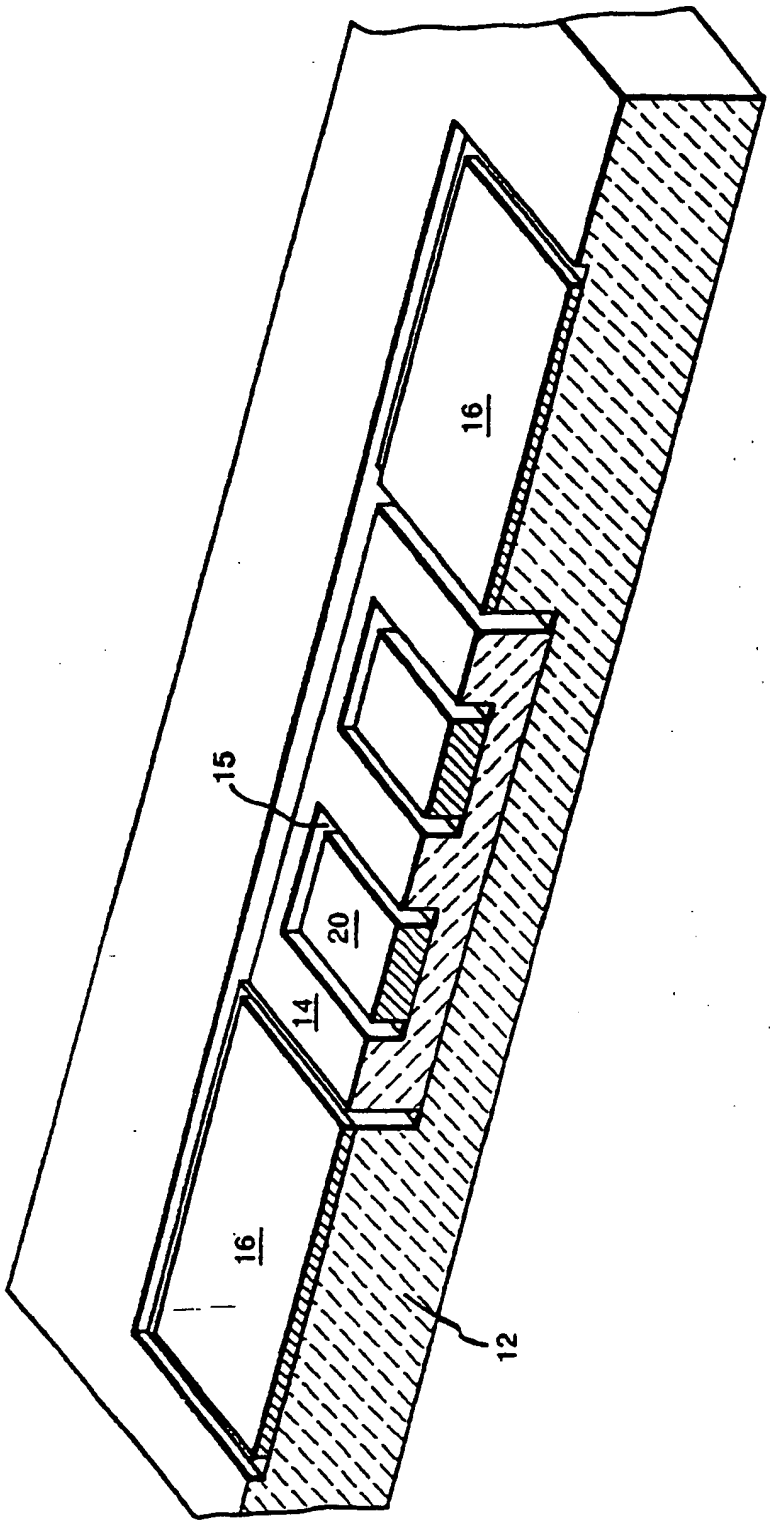


FIG. 4

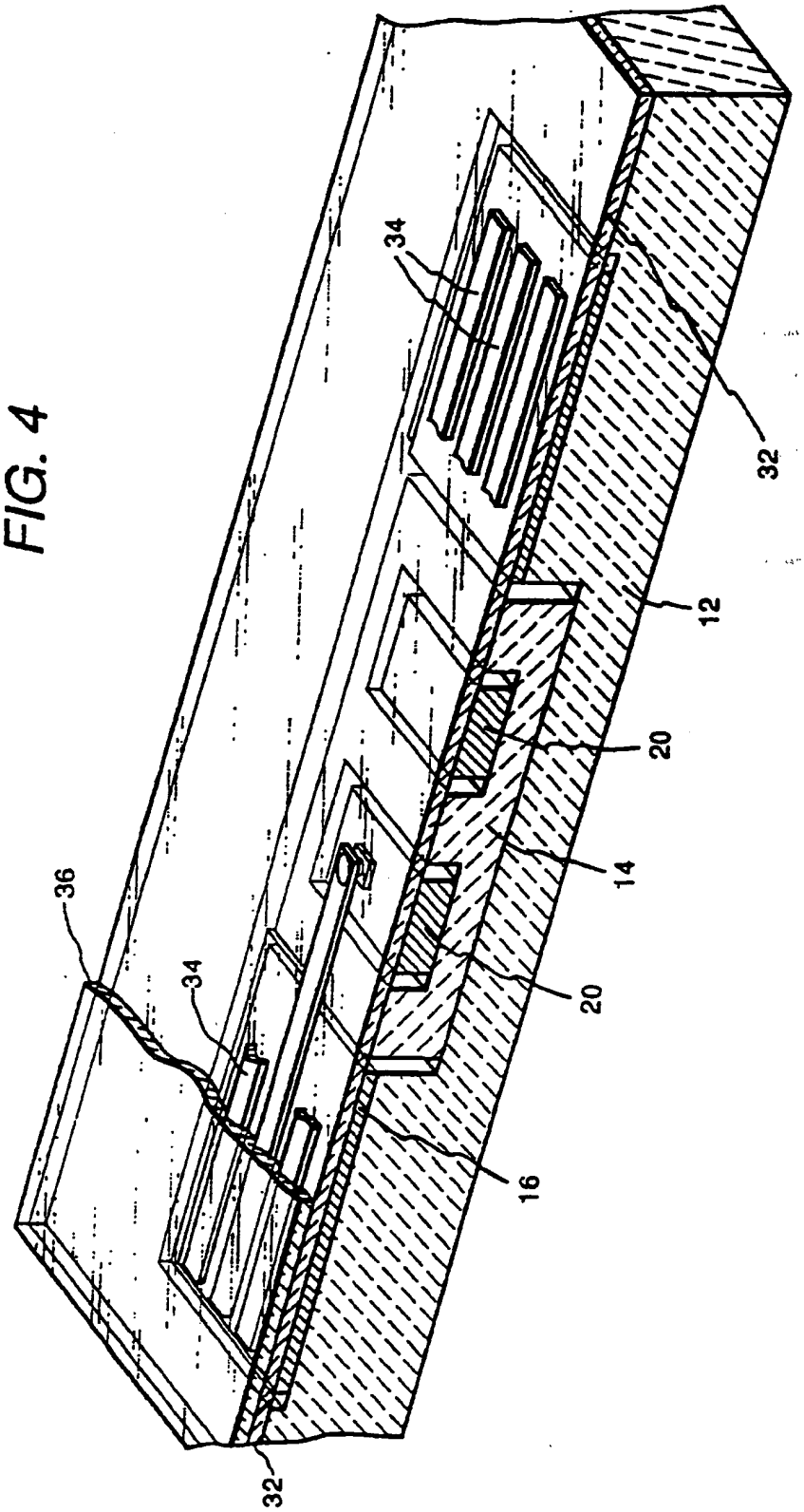


FIG. 5

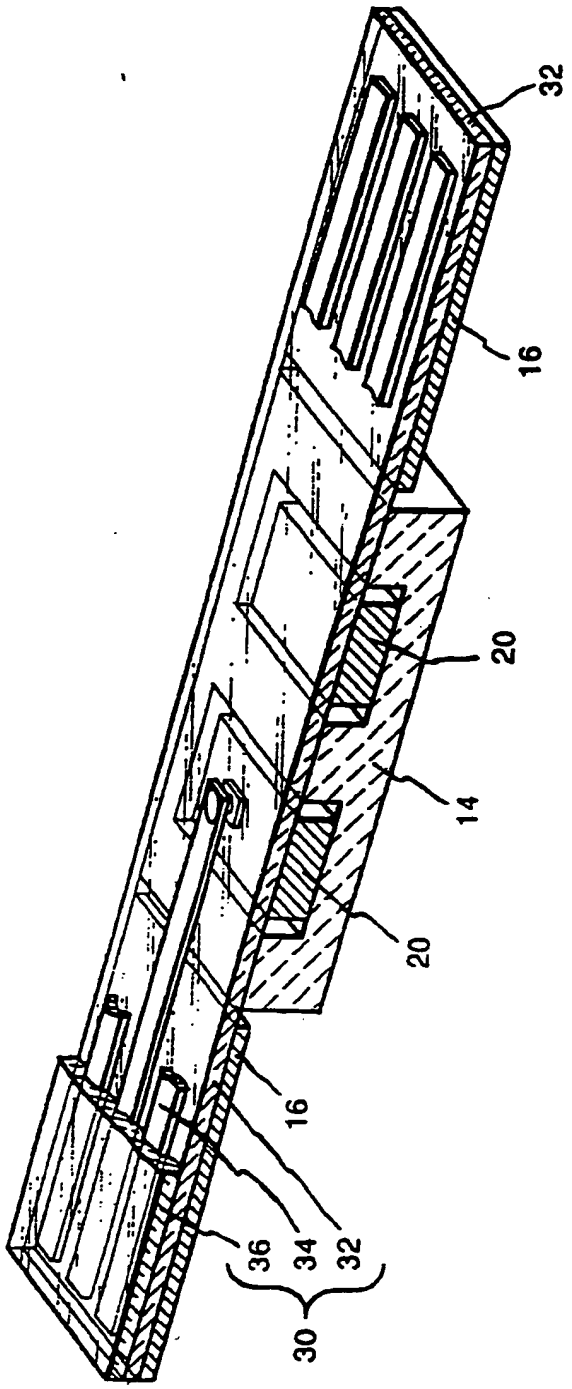


FIG. 6

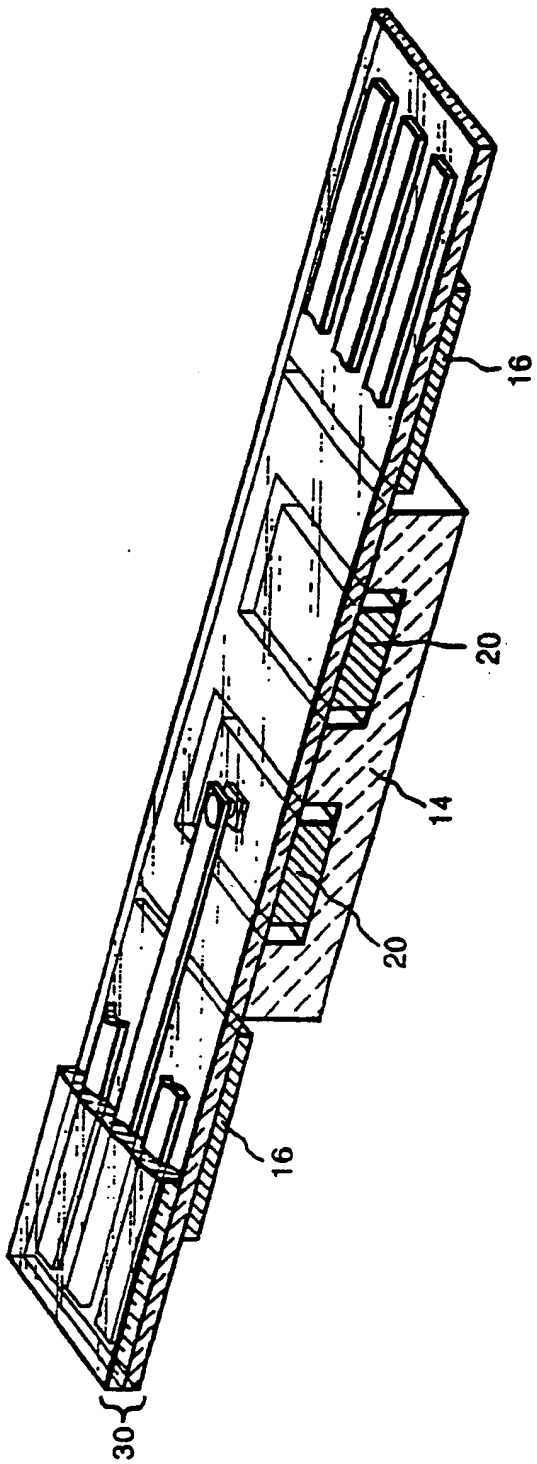
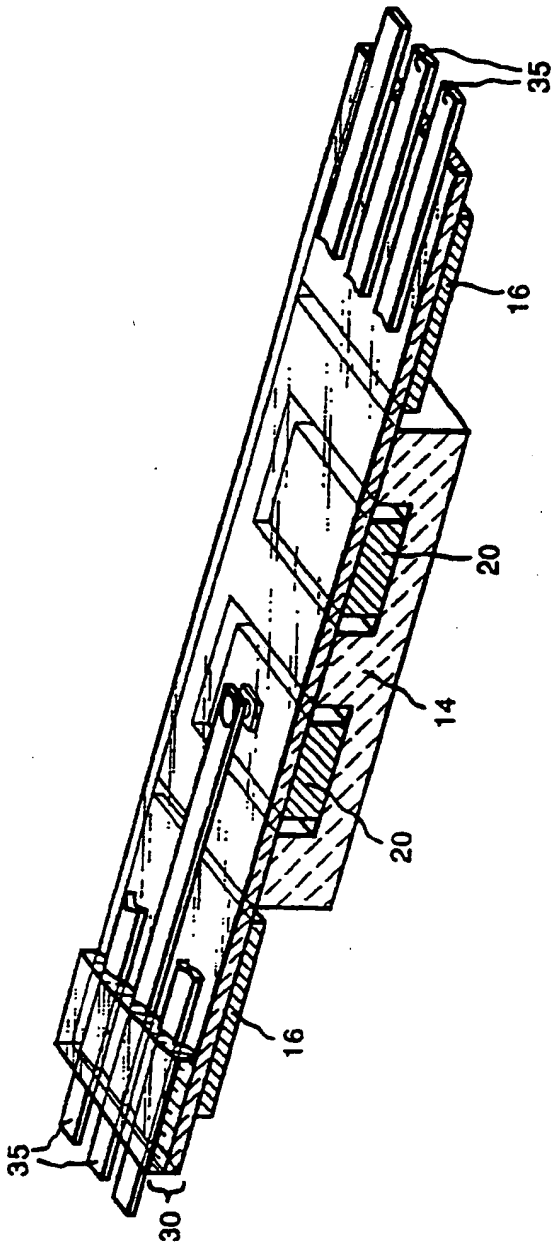


FIG. 7



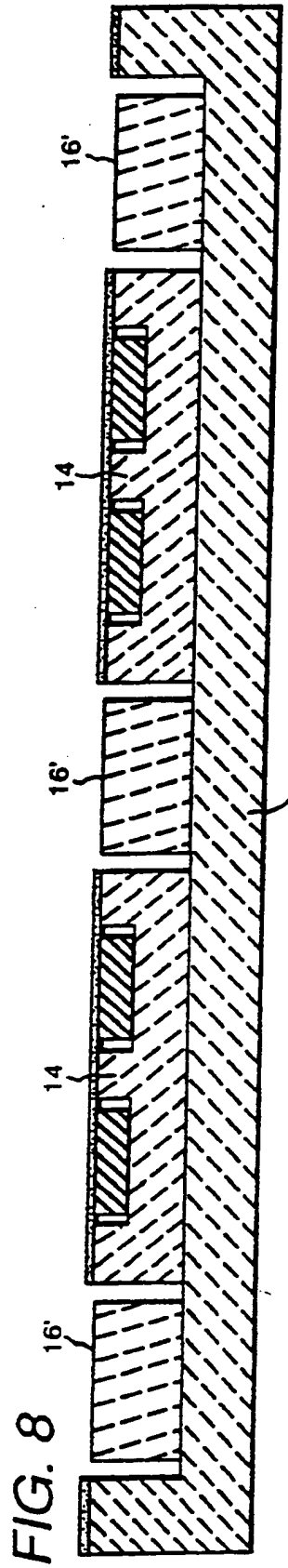


FIG. 8

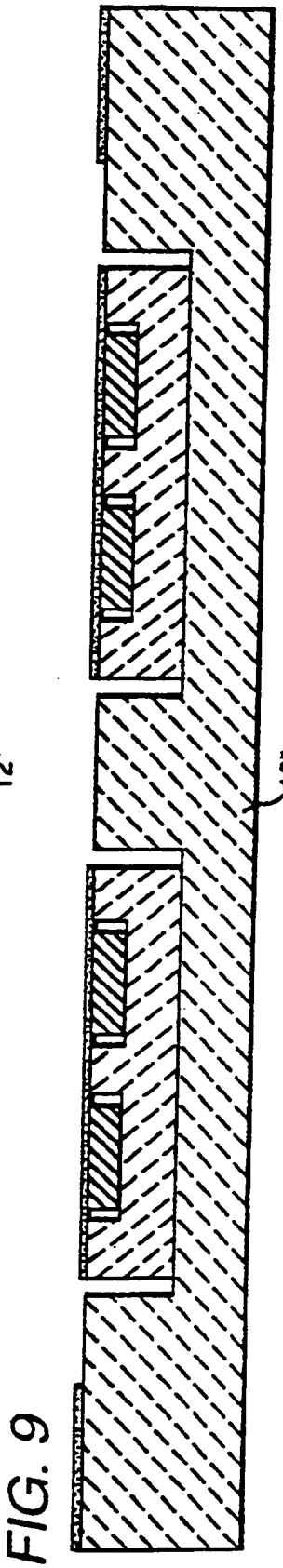


FIG. 9

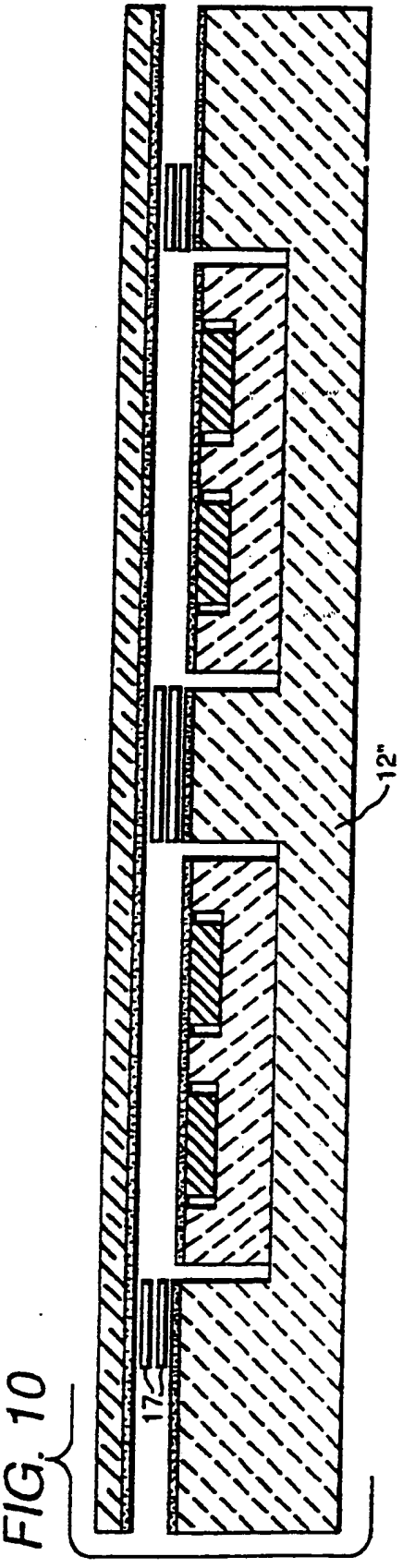


FIG. 10

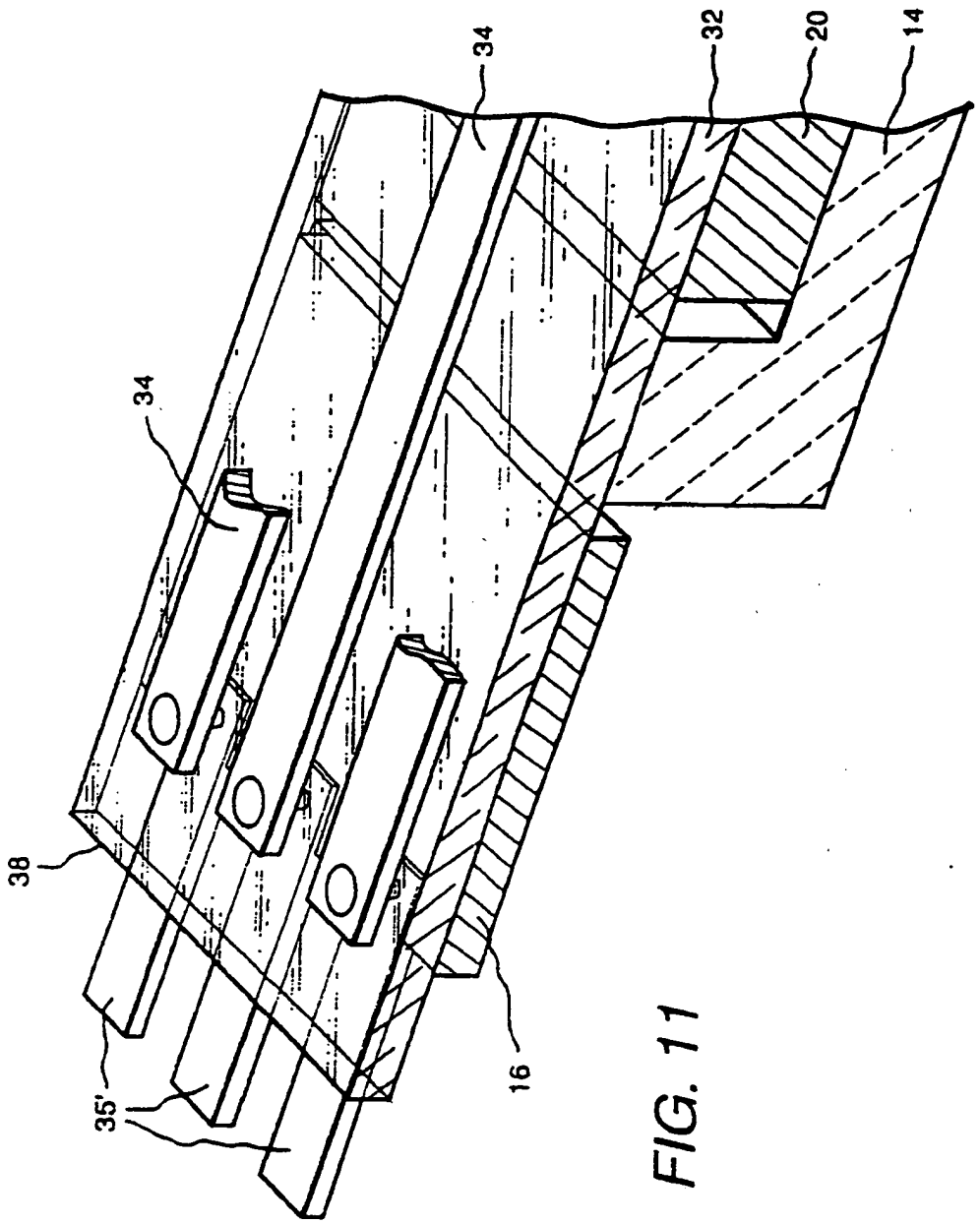


FIG. 11

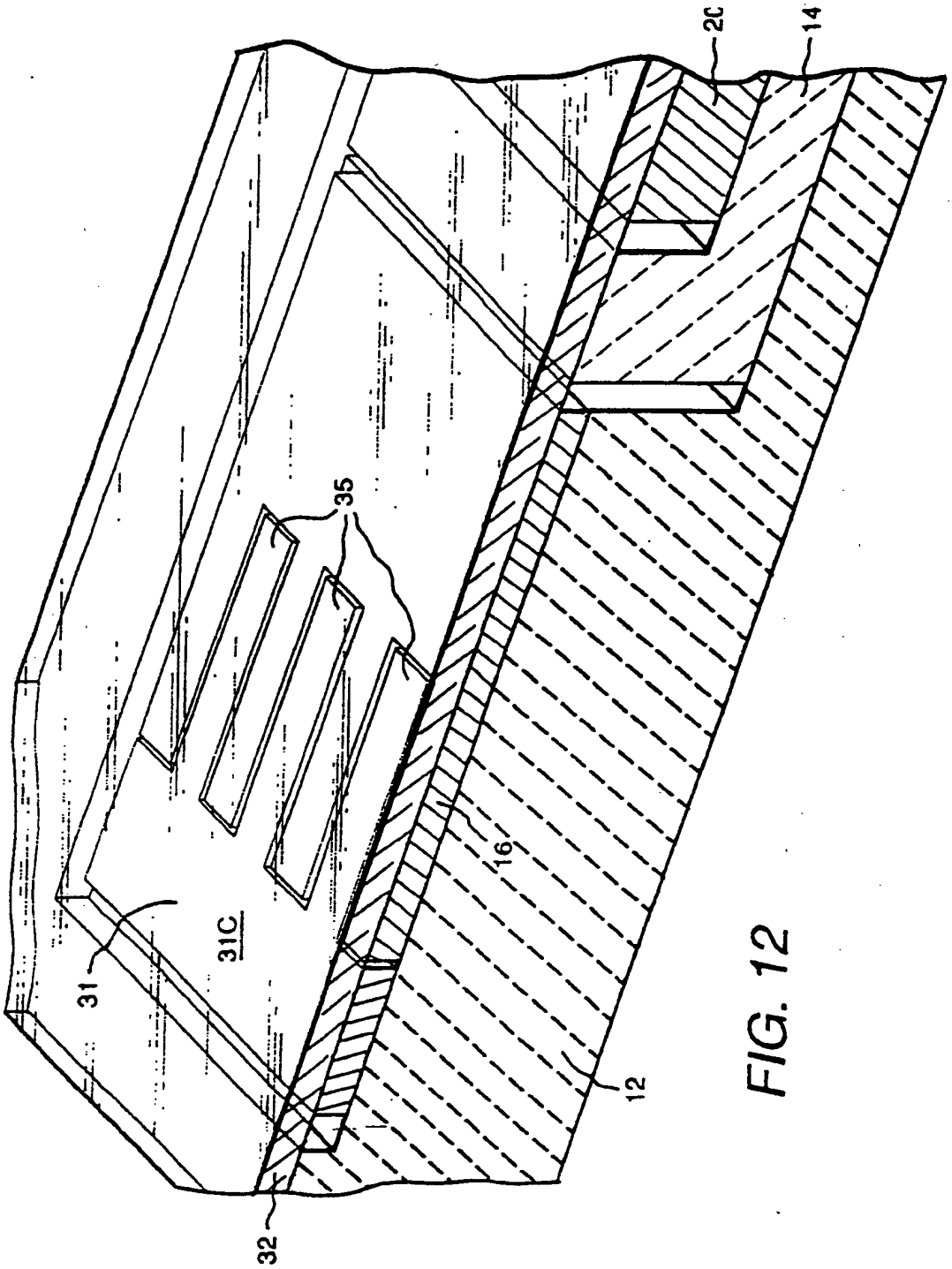


FIG. 12

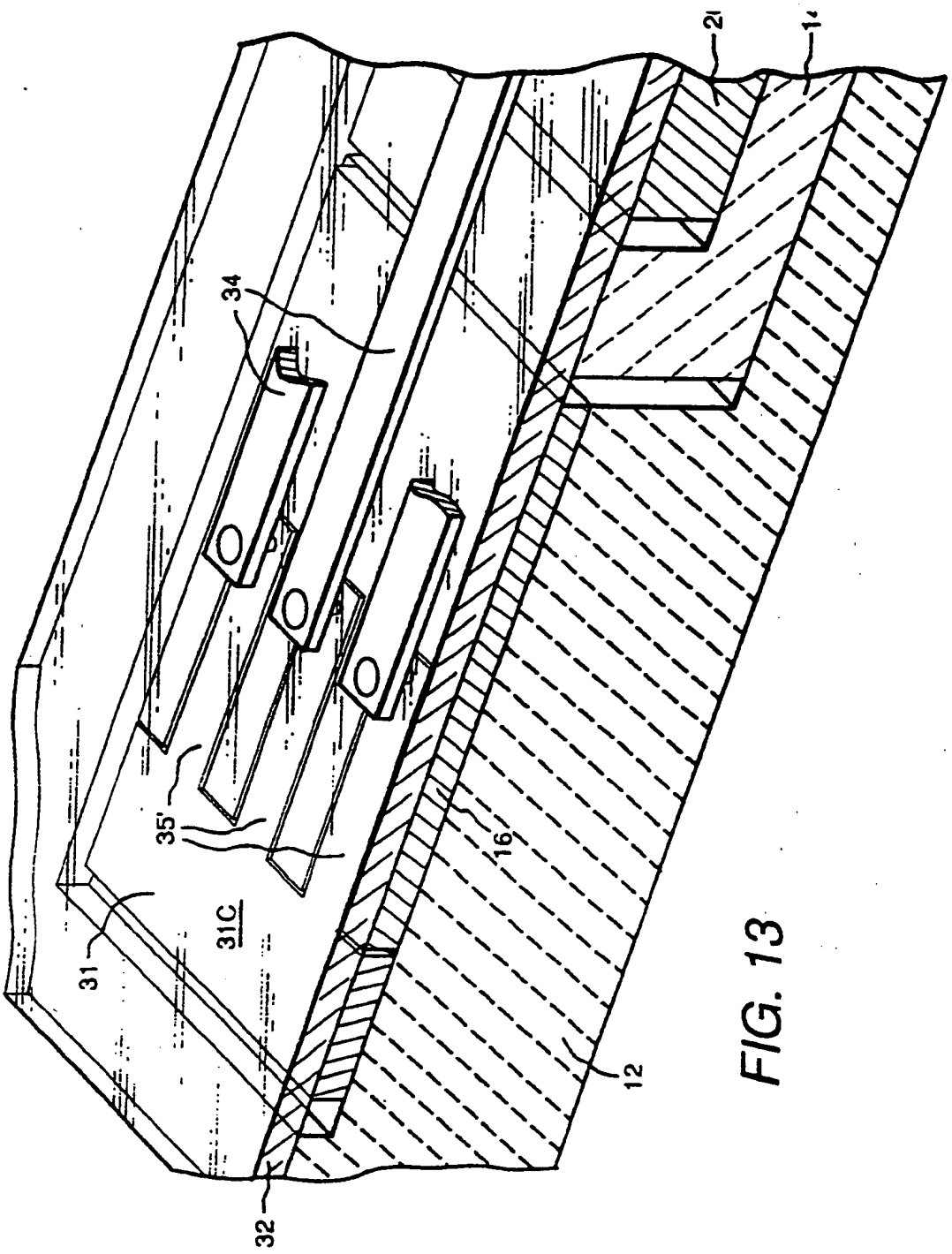


FIG. 13

FIG. 14

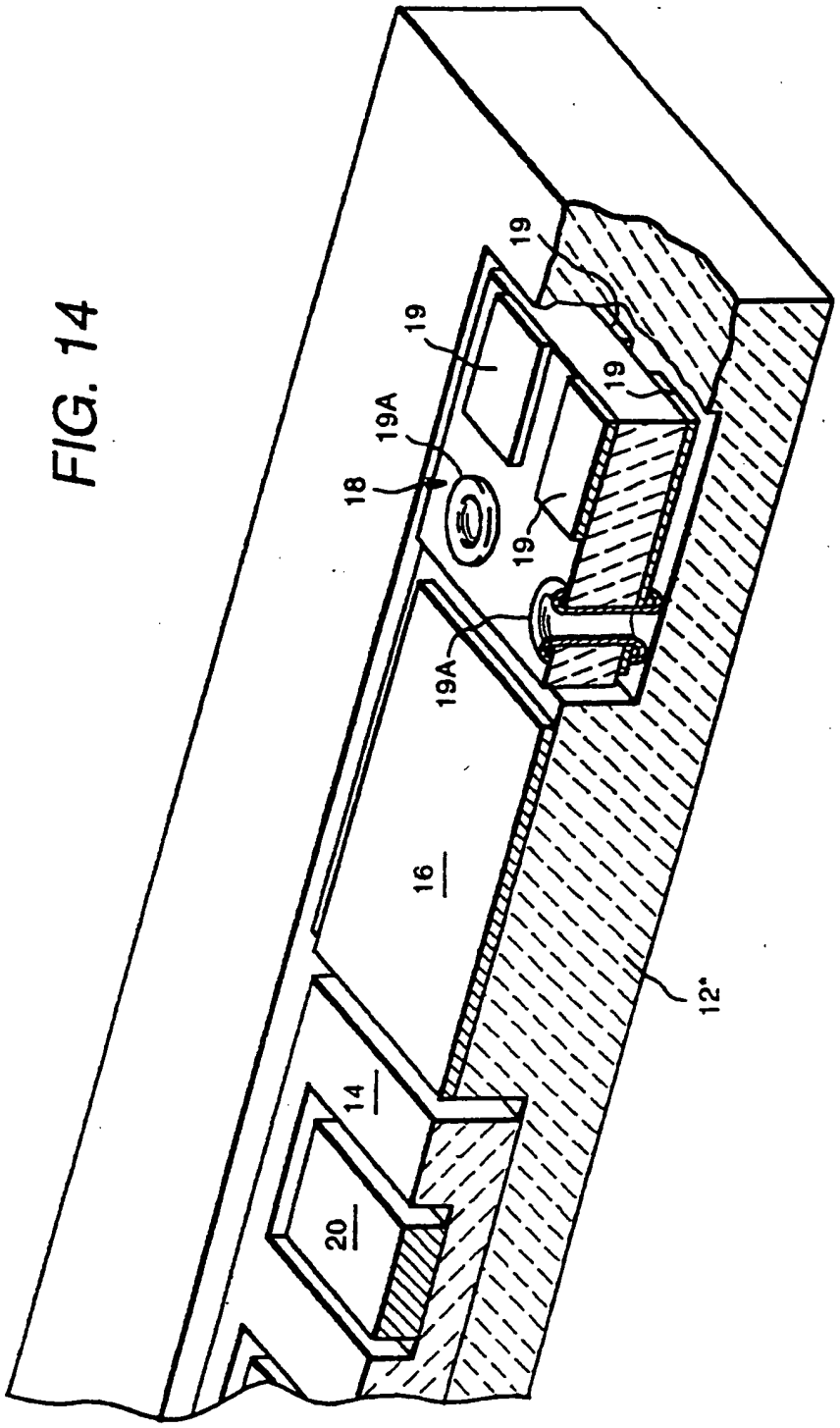


FIG. 16

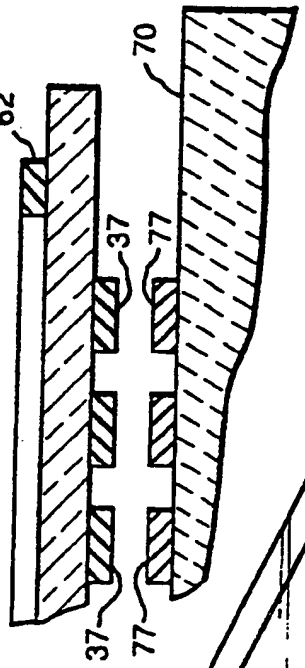
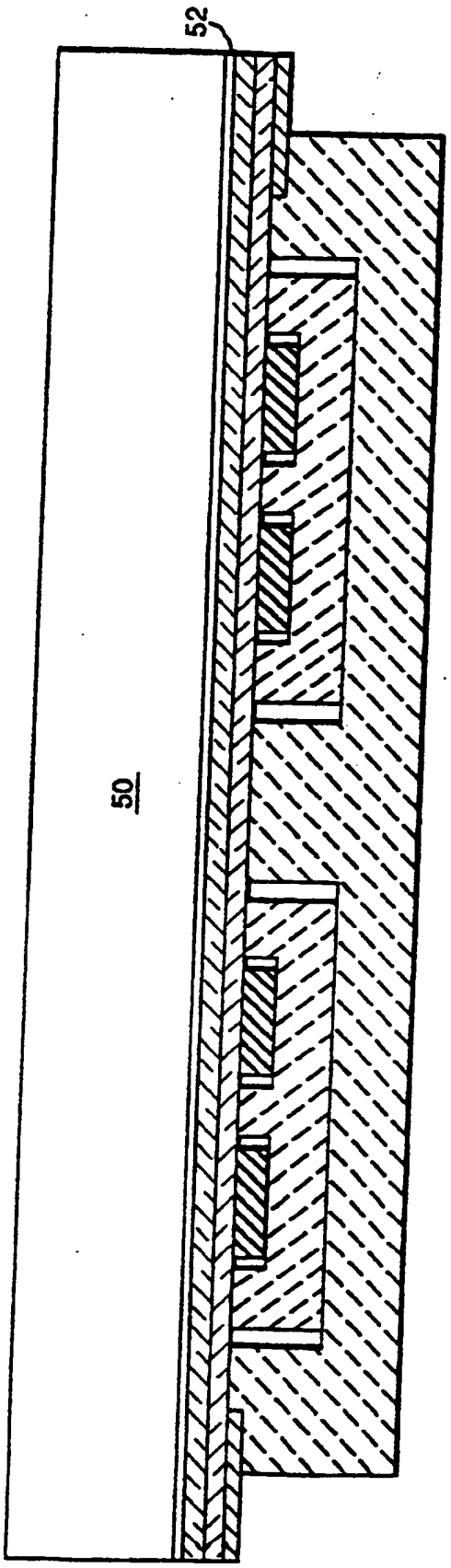


FIG. 15

FIG. 17



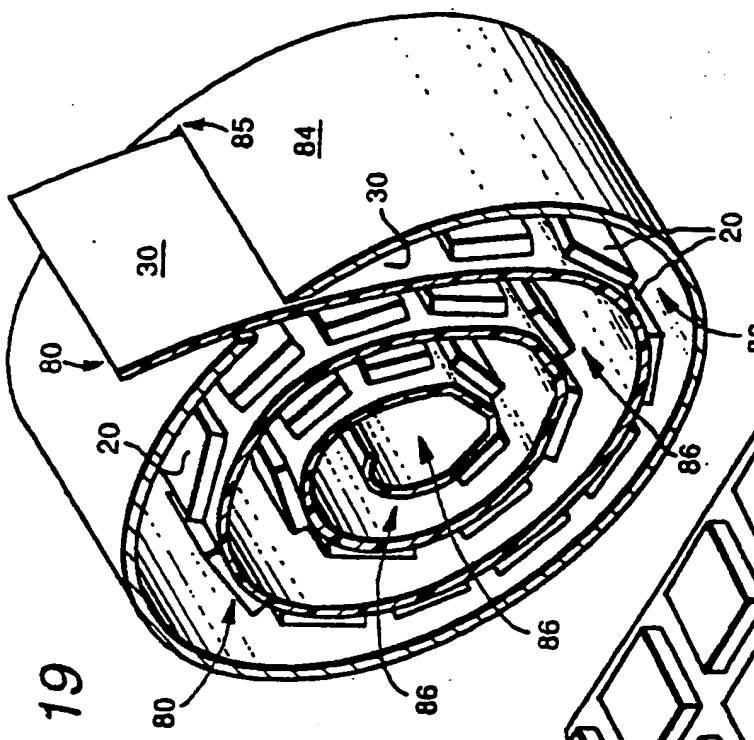


FIG. 19

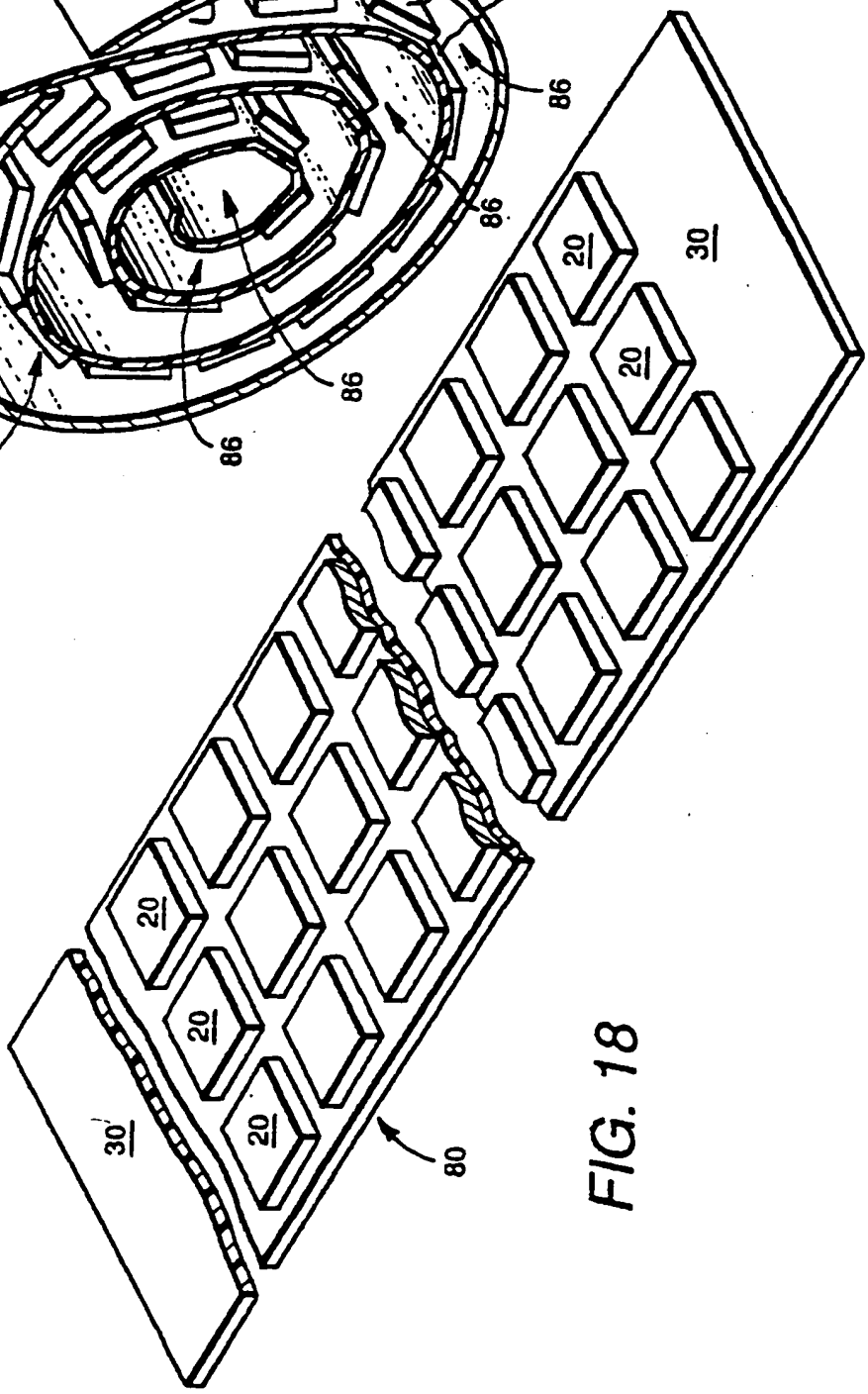


FIG. 18